REMARKS

As a preliminary matter, because each of the outstanding rejections is a mere repetition of the rejections from the previous Office Action, Applicants incorporate by reference herein all of those arguments presented in Amendment M, filed April 24, 2006. Applicants respectfully request that the Examiner reconsider those remarks, and withdraw all of these rejections. The following arguments therefore, are primarily focused on the Examiner's new remarks, as well as several of the significant deficiencies that still appear in all of the outstanding rejections.

For example, with respect to the repeated Section 112 rejection of claims 1 and 14-16, the outstanding Office Action fails to assert or indicate how any one skilled in the art would interpret the drawings of the Specification according to only the Examiner's personal, and highly restricted, interpretation. The rejection also still fails to cite to a single drawing or text portion from the present Application that defines a data bus line (or element 22) to be only that portion of the line on the side of the switches (element 66 in Fig. 7, for example) that is opposite to the liquid crystal panel 16, as the Examiner erroneously continues to assert. None of the drawings cited by the Examiner designate the lines 22 by a different number on different sides of the elements 66, as the Examiner appears to imply, and no evidence has been submitted to show that any person of ordinary skill in the art would so interpret these drawings. In fact, the present Specification directly contradicts such an interpretation.

Page 1, lines 32-35 of the present Specification expressly states that the display signals "are applied to the liquid crystal panel 16 via the data buses 22." The Examiner

himself even cites this portion of the Specification, yet still somehow concludes that the data bus lines 22 cannot extend to the liquid crystal panel 16, despite of this clear description on page 1 of the present Specification that says the data bus lines are applied to the liquid crystal panel. This portion of the present Specification that the Examiner himself has relied upon is the very portion that defeats his asserted Section 112 rejection. The Examiner's request that Applicants must show additional evidence to overcome this rejection is therefore meritless.

The Examiner has the burden to establish where one of ordinary skill in the art would find the cited language from the present claims confusing when these claims are read in light of the present Specification. This burden, however, has not been met. The very drawings and text cited by the Examiner from the present Specification all clearly support the cited claim language. All of these drawings unmistakably show the data bus lines coming from the display panel and connecting to the signal lines via ("by way of") the analog switches. The Examiner has submitted no evidence, however, whether from the prior art or the present Application, to contradict these clear teachings. The Examiner's assertion therefore, that "the instant Specification defines what constitutes a '*data bus line*' in direct contradiction to what is being claimed" (page 12, lines 9-11 of the outstanding Office Action, emphasis in original), is clearly erroneous.

Furthermore, although the Examiner is considered to have skill in the art, his own personal knowledge, experience, or understanding is not a basis upon which the claims may be rejected. See In re Lee, 277 F.3d 1338, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002). The fact that the Examiner may himself be confused is also not, by itself, sufficient to establish a

rejection under Section 112. Applicants have repeatedly demonstrated how the Examiner has misinterpreted the drawings and the text of the present Application. These arguments have not been rebutted, and no portions of the present Specification have been identified to support the Examiner's assertions that his interpretation of the drawings is even correct, let alone the only correct interpretation. It is highly inappropriate for the Examiner to simply continue to repeat this same rejection without first attempting to actually answer any of the arguments that prove the rejection to be unfounded. Accordingly, the Section 112 rejection is still without merit, and must be withdrawn.

The repeated Section 102 rejection of claims 1-6, 8-16, and 18-21, and the Section 103 rejection of claims 7 and 17, present similar deficiencies to those discussed above regarding the improper Section 112 rejection. Whether or not a rejection is based on either anticipation or obviousness, the Examiner is nevertheless still required to show where the prior art teaches (or suggests) each and every claimed feature and limitation, or a *prima facie* rejection simply cannot be established or maintained. In the present case, this burden still has not been met.

Applicants have repeatedly demonstrated how none of the cited portions from the Nakajima reference (U.S. 5,654,735) teach or suggest any of the features of the present invention regarding the simultaneous supply of signals to the other recited elements in the claims. Remarkably, however, the Examiner continues to assert (page 4, last five lines of the outstanding Office Action) that Nakajima somehow discloses such features. Nakajima, however, simply does not. The only simultaneity ever described by Nakajima is with respect

to the *sampling* of the video signals SIG1, SIG2, SIG3, and not the supply of these signals to other elements. Over many Responses now, the Examiner has still never cited to one single instance of a simultaneous supply of signals, or more particularly, of any of the signals featured in the present invention.

The Examiner's remarks regarding Applicants' most recent arguments fail to take into account the Examiner's own original remarks that prompted Applicants' arguments. The Examiner is the one who stated that the simultaneous transmission features of the present invention are "little more than the *inherent result* of the signal lines [Fig. 7; 74A] and the data bus lines [Fig. 7; 68] being connected to one another." This assertion was improper both for failing to establish the asserted inherency (the cited portions of the present Specification in no way support the assertion), *and* for demonstrating an impermissible use of hindsight (for relying only upon the present Application as the only support for claim features that have not been cited in any prior art reference). The Examiner was not requested to choose between which of these arguments to answer. The rejection was improper for both reasons, and the Examiner was therefore obligated to answer both arguments, or withdraw the rejection. Neither argument is answered by the Examiner's claim that he cannot choose which one to answer.

The Examiner's additional assertion, that "'inherent results' have more to do with the laws of nature rather than any particular hindsight teachings within the present Specification," also failed to answer any of Applicants' arguments that challenged this assertion of inherency. What may or may not be inherent in nature is irrelevant to whether

the Examiner has met the MPEP's clear requirements to establish that a case of inherency even exists. The Examiner may not just simply assert that inherent results exist. The Examiner is instead required to prove that such results must occur, with objective evidence on the record, and particularly when the assertion of inherency was timely challenged by Applicants. In the present case though, Applicants did challenge the assertion of inherency in a timely manner, but the Examiner has failed to support his assertions with any required evidentiary showing on the record. Accordingly, the asserted cases of both anticipation and obviousness are deficient on their faces, because both rely upon this unsupported assertion of inherency.

Both of the stated grounds for rejection are further deficient because the prior art does not support the Examiner's substantive assertions either. The Nakajima reference simply fails to teach or suggest that display signals are supplied from the signal lines to the blocks of the display panel via analog switches simultaneously with the supply of display signals to subsequent blocks of the panel. It is well known in this field of art that *timing* considerations are not automatically inherent to any two elements merely being connected to each other. Signals can be supplied continuously, intermittently, selectively, or delayed, even between two such directly connected elements. The Examiner has alleged nothing more than the fact that two particular elements of the present invention are connected. His additional conclusion, that signals between any of these elements are inherently simultaneous, is not taught or suggested by any of the cited portions of Nakajima, nor is it supported by any disclosure within the present Specification.

Again, Applicants have repeatedly pointed out on the record that the only simultaneity taught by Nakajima is the *sampling*, and not the supply of the signals themselves. Applicants have further pointed out how Nakajima repeatedly teaches how the supplied signals are actually only sequential, held, or delayed, but not simultaneous. These arguments, all of which directly challenge the original *prima facie* cases asserted against the present invention, have been repeated over many Responses, and never rebutted or answered. The selective challenge to only some of Applicants' arguments in rebuttal to a potential *prima facie* case does not answer any of these arguments that directly traverse the *prima facie* cases themselves.

The asserted *prima facie* case is further deficient in its stated interpretation of the Nakajima reference itself. The Examiner asserts that Nakijima's video signals SIG1-SIG3 and sampling pulses Φ_{n-n+2} are somehow analogous to the data bus lines of the present invention, and that Nakajima's data line potentials V_{n-n+1} are somehow analogous to the signal lines of the present invention. These assertions are without any merit. One of only ordinary skill in this field of art would easily know that video *signals* (col. 4, line 23) and sampling *pulses* (col. 4, lines 35-36) simply are not the same as the lines that carry such signals and pulses. The Examiner has not cited any teaching or suggestion from Nakajima that supports his assertion that signals carried on a line are equivalent to the line itself.

Nevertheless, even if this assertion by the Examiner were reasonable (which it is not), the Examiner's attempt to label such signals and pulses as equivalent to the data bus lines of the present invention is directly contradicted by the Nakajima reference itself.

Nakajima expressly states that the data lines Y are those vertical lines that intersect the mutually orthogonal and horizontal gate lines X in the display panel 1, and the individual pixels 11 are arrayed at such intersections. (Col. 4, lines 4-6; Fig. 1). The Examiner's assertion therefore, that the signals SIG and pulses Φ could somehow represent the data lines simply makes no sense, because Nakajima clearly teaches that this completely different portion of the device (lines Y) comprises the data lines.

Applicants further note for the record here that Nakajima's unambiguous illustration of the data lines Y also directly contradicts the Examiner's other assertions, as discussed above. Nakajima clearly shows in Fig. 1 that the data lines Y extend all the way into and through the display panel 1. Nakajima does not teach, or even suggest, any separate designation for the data lines Y on different sides of the switches HSW.

The Examiner appears to have made a similar mistake in attempting to assert that the voltage potentials V are analogous to the signal lines of the present invention. Not only does Nakajima fail to support this assertion, Nakajima directly contradicts it. Nakajima clearly teaches that the symbols V_{n-n+1} designate the actual voltage potentials of the respective data lines Y. (Col. 6, lines 45-46, 55-56). Similar to the problem noted above, one of ordinary skill in the art would also easily know that voltage potential is not the same thing as signal line that may hold such a potential. And even if such an assertion did have any merit (which it does not), it still would make no sense to additionally assert that the voltage potential of a data line Y somehow can be a *signal line*. The Nakajima reference has thus been clearly misinterpreted.

One of ordinary skill in the art can easily see that Nakajima does show signal lines, as the term is well known in the art, in Fig. 1. A simple comparison with any of the relevant drawings from the present Application shows that only the four horizontal lines at the top of Nakajima's horizontal driving circuit 13 (above the switches HSW) could be analogous to the recited signal lines of the present invention. The Examiner has not cited one teaching or suggestion from Nakajima that would contradict this fact.

Moreover, even were the Examiner's analogies to the present Application somehow meritorious, Applicants are nevertheless at a loss to understand the Examiner's additional assertion of "the number of the data bus lines [SIG1-SIG3, Φ_{n-n+2}] being larger than a number of the signal lines [V_{n-n+1}]." As cited by the Examiner, Fig. 1 of Nakajima shows only three video signals SIG and three sampling pulses Φ, but nine total voltage potentials V. Applicants simply cannot understand how the Examiner can be asserting that six lines (three plus three) is larger than nine lines. Accordingly, the outstanding Section 102 and 103 rejections based in whole or in part on Nakajima must be withdrawn.

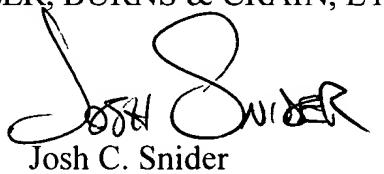
Although no further amendments are necessary to place all of the present claims in condition for immediate allowance, Applicants have nonetheless attempted to add one more clarifying amendment to the independent claims of the present invention in the hopes of helping the Examiner understand this field of art, and the present invention and the Nakajima reference in particular. Specifically, Applicants have emphasized how the number of data lines relative to the number of signal lines are those <u>included within each block</u> in the present invention. Although such features should have already been implicit when the

present claims were read in light of the Specification, Applicants submit this additional clarification of the claims in the hopes that the Examiner will be better able to distinguish between the various different elements and functions within the cited Nakajima reference.

For all of the foregoing reasons, Applicants submit that this Application, including claims 1-21, is in condition for allowance, which is once again respectfully requested. The Examiner is invited to contact the undersigned attorney if a further interview would help expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

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October 11, 2006

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